National Yang Ming Chiao Tung University's Successful Challenge to the Next-Generation Angstrom-Level Integrated Circuit Technology, with Potential to Go "More than Moore"

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With the rapid advancement of semiconductor technologies and the industry in recent years, the concept of a monolithic three-dimensional integrated circuit (M3D-IC) has emerged as a solution to overcome the limitations of transistor miniaturization, as predicted by Moore's law. M3D-IC technology involves a shift toward a multilevel vertically stacked structure in transistors, allowing for increased transistor density within a limited chip area and aiming to achieve "More than Moore." This technology is expected to enable the production of small chips with high processing speeds and low costs while further miniaturizing semiconductor manufacturing processes.

Led by Liu Po-tsun, a Chair Professor from the Department of Photonics at National Yang Ming Chiao Tung University, a team conduct the National Science and Technology Council's Angstrom Semiconductor Initiative in an international collaboration with Professor Kuo Yu at Texas A&M University in the U.S., who is also a Yushan Fellow. The team focused on innovations in materials, transistor devices, and circuits, leading to the development of a complementary field-effect transistor (CFET; Figure 1) specifically designed for use in M3D-ICs. They employed a novel semiconductor material called amorphous indium tungsten oxide (a-IWO) to achieve exceptional current performance in the channel with a thickness of only a few atomic layers. The CFET also exhibited high voltage gains in logic circuits, low static power at the pico-watt level, and a highly symmetric noise margin (see Figure 2). By successfully addressing the technological challenges associated with M3D-IC, the team's novel material and technology proved comparable to the silicon-based transistor commonly used in the semiconductor industry today.

The technological advancements achieved through this research hold significant application value for next-generation Angstrom-level integrated circuits; it facilitates the integration of heterogeneous semiconductor chips that contain high densities of transistors, while achieving high device performance with low power consumption. This milestone represents a significant breakthrough for the semiconductor industry beyond the scope of Moore's law. The research finding has also been published in the prestigious journal ***Advanced Science*** (p. 2205481, Jan. 2023. Impact Factor: 17.52, FWCI: 3.32).

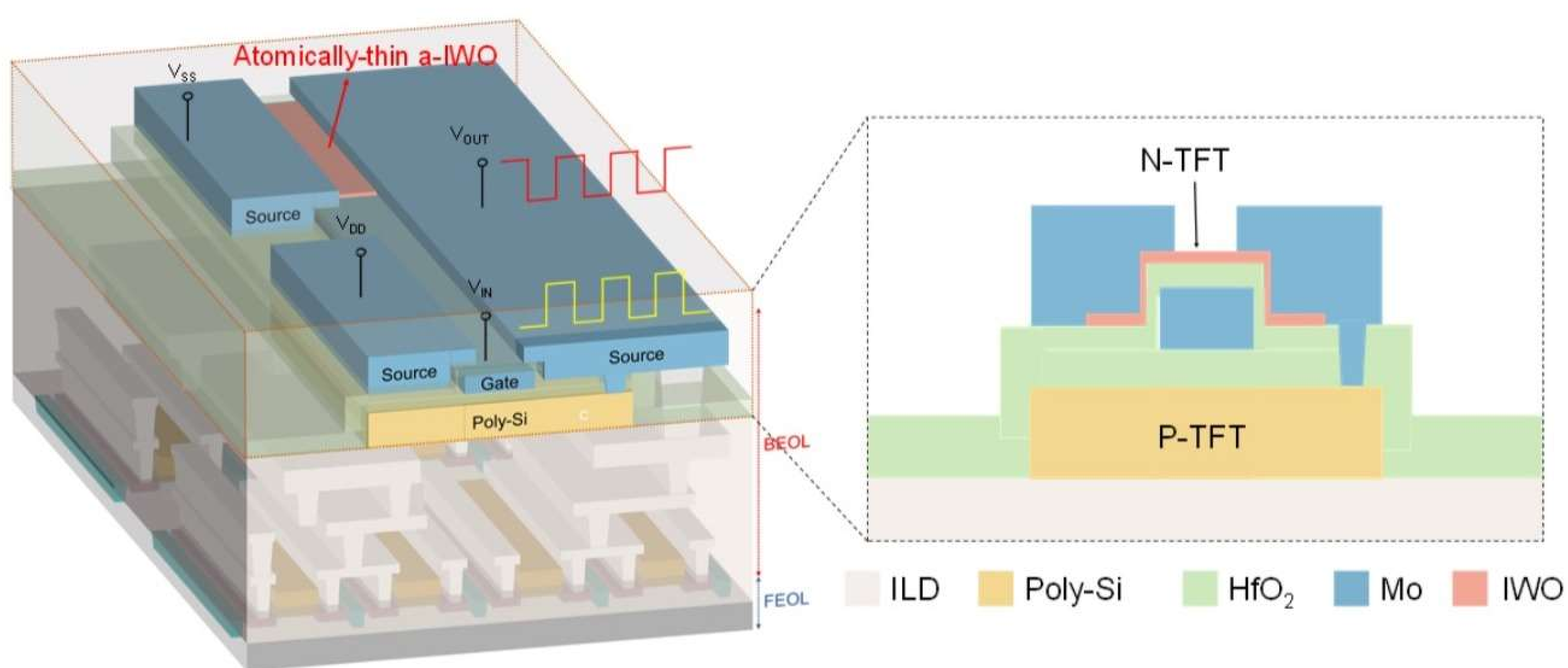

Figure 1. The vertically stacked CFET structure for use in M3D-ICs to facilitate the manufacturing of advanced semiconductor chips with ultra-high densities of circuits.

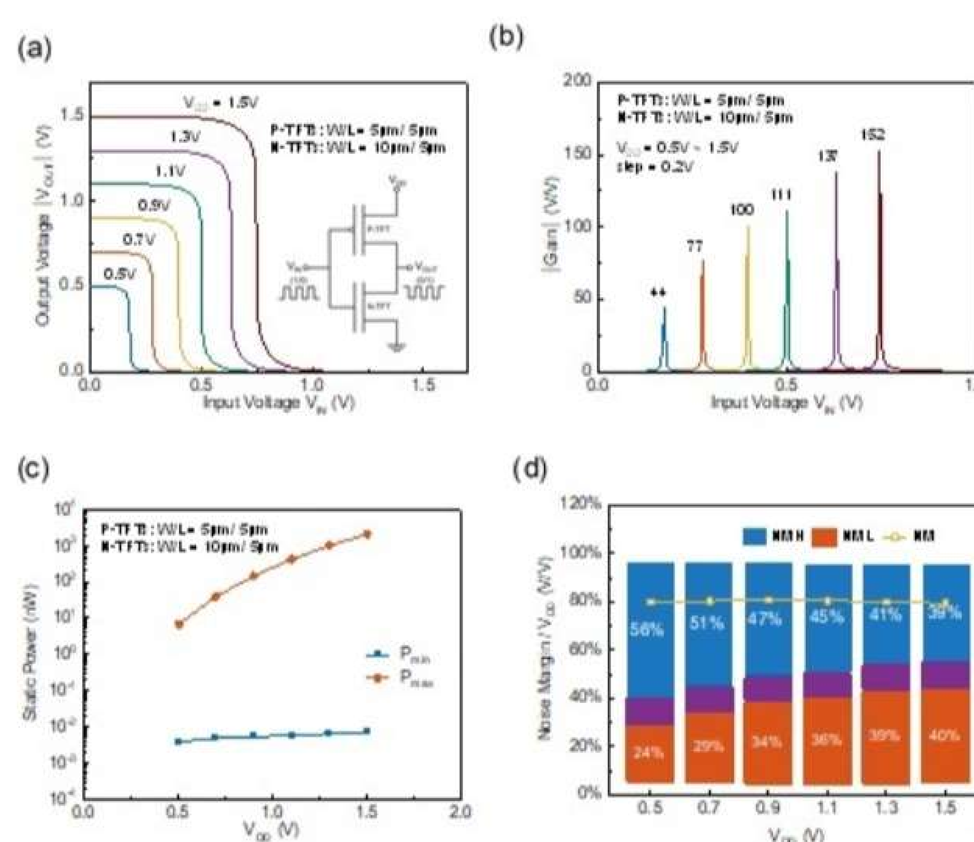

Figure 2. The performance of an inverter comprised of three-dimensional vertically stacked CFET at various operating bias voltages: (a) low-bias-voltage transfer characteristics, (b) high-voltage gains (~ 152V/V), (c) ultralow static power consumption at the pico-watt level, and (d) highly symmetric noise margin (~80%).

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